Review of Wide Bandwidth Noise Amplifier for Modern Wireless Communication

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Abstract— Recently, the rising the demand of Low Noise Amplifier (LNA) products for the high data rate communication system. LNA transistors are used in applications where a high gain and noise rejection is needed. Recently Low Noise Amplifier (LNA) products have been reported high gain and good bandwidth for modern application. In modern communication Low Noise Amplifier (LNA) products is versatile used in low noise amplifier, distributed amplifier, broadband mixer, power amplifier and active balunes. Today technology required high speed transmission efficiency with less power consumption and less circuitry to used, Low Noise Amplifier (LNA) products satisfy all parameters so that review and future advancement required. In these papers designing, application, issues and recent trends of Low Noise Amplifier (LNA) products is reviewed; we have surveyed almost all the Possible Work Done in Low Noise Amplifier (LNA) products in Past Decades.

Keywords—Ultra-wideband (UWB), Hetero junction bipolar transistor (HBT), high electron-mobility transistor (HEMT), MOS Varactor, Narrow energy material.

I. INTRODUCTION

CONTINUOUS scaling of CMOS technology keeps driving the innovation of RFICs with higher integration level and lower cost. Significant efforts on the study of both devices and circuits also substantiate the wireless communication systems operating toward higher frequencies. Using the K-band (18 – 26.5 GHz) for short-range and high data-rate wireless communication and anti-collision radars is recently of great interest to both industry and academia [1]–[6].

Similar with other portable wireless applications, low-power design is a critical Issue [6]. In this letter, we present an ultra-low-power 24 GHz low-noise amplifier (LNA) in 0.13 CMOS technology. A peak gain of 9.2 dB and a minimum noise figure of 3.7 dB are achieved with a DC power consumption of 2.78 mW only. Design of RF LNAs consists of two major parts, namely selection of transistor geometry and bias point, and also determination of circuit topology including the matching networks. The characteristics of transistors play a critical role, since the core circuit is composed of only a few transistors in most cases. In addition, a simple circuit topology is often preferred to prevent the unpredicted parasitic effects from the complicated layout.

II. REVIEW OF TECHNIQUES

A. *Wide Range Derivative Superposition Technique*

This technique presents an L-band highly linear differential low noise amplifier (LNA) in a standard 90-nm CMOS process. A wide range derivative superposition technique is used to maximize the third-order intercept point (IP3), and at the same time, minimize the third-order inter-modulation distortion (IMD3) over a wide-input power range.

B. *Direct-Coupled Amplifier Topology [2]*

A schematic of the direct-coupled amplifier is shown in Fig. 1. This topology has previously demonstrated sub-2.5 dB noise figure and 3-dB bandwidths up to 6 GHz [l]. The direct-coupled amplifier topology consists of two gain stages. The first stage is a common-emitter amplifier comprised of a 2 x 10pm2 HBT transistors, Q1. The second stage is a feedback amplifier comprised of 2 x 10 pm2 HBT Darlington connected transistors, *Q2* and *Q3,* series feedback resistor *Re,,* shunt feedback resistor R f **1** , bias resistor load resistor ***Rload,*** and output matching resistor *Rout.* Transistors Q1 and *Q3* are nominally biased at a collector current of **4** mA while transistor *Q2* is biased at a collector current of 2 mA. The first stage acts as a low noise common emitter amplifier stage

which determines the noise figure of the overall 2-stage amplifier. The second stage Darlington feedback amplifier provides wideband gain and output drive capability. The bandwidth characteristics of the Darlington feedback stage can therefore be optimized by changing the series and parallel feedback resistors without degrading the noise figure of the overall amplifier. The shunt feedback resistor R fi of the Darlington stage can be adjusted for gain bandwidth performance. Rfi also provides a current source for biasing transistor Q1 of the first stage. The shunt feedback resistor, R f2, connected between the emitter of transistor *Q2* and the base of transistor Q1, can be adjusted to change the effective impedance

looking out of the base of transistor QI toward the source, and therefore, optimized for minimum noise

match. In addition, Rf2 provides rf shunt feedback, which impacts the gain-bandwidth response and determines the input impedance match of the amplifier to 50 R. Thus, feedback resistor Rf2, can be adjusted to obtain optimal noise figure as well as input return-loss performance.
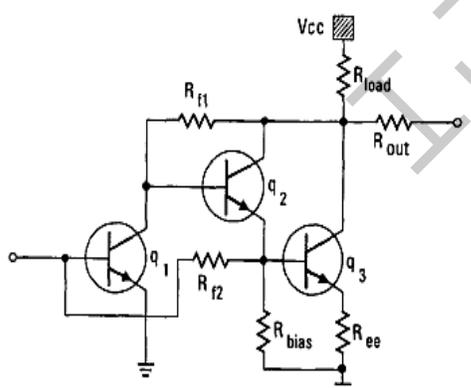

Fig. 1. Schematic of the direct-coupled HBT amplifier.

C. *Resistive shunt feedback topology and Matching T-network sections*

Broadband systems have traditionally employed distributed amplifier topology. The problem of achieving a broadband match to the transistor input and output impedance is overcome by incorporating the input and output capacitances of a number of transistors into artificial transmission-line structures. But recently, for UWB system, the low power consumption requirement imposes a great challenge on low power distributed amplifier design. And also for distributed amplifier, there is a 50- termination resistor in front of the first stage of the amplifier; this will degrade the noise performance of the distributed amplifier substantially. In the proposed solution, shown in Fig. 1, the input stage of the LNA was designed by employing a resistive shunt feedback topology together with two T-network sections to match to a 50- antenna. At the same time this topology will improve the noise performance compared to the distributed input stage. The second stage is implemented in common source configuration to achieve the higher gain compared to common gate configuration. Current sharing design of the two stages is employed to reduce the power consumption of the proposed LNA under fixed 3-V battery [5]. The output matching is achieved by a single transistor distributed amplifier topology, which means that the inductors absorb the output capacitance of the second pHEMT to form an artificial transmission line terminated by 50- to drive an external 50- load.
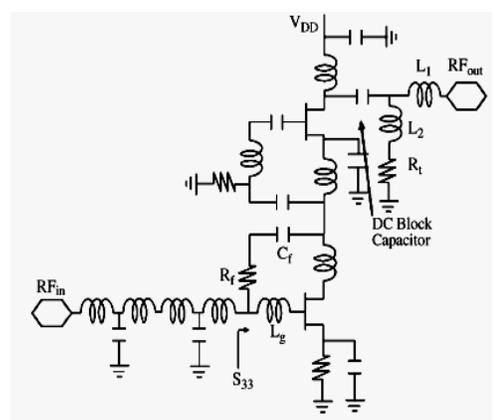

Fig. 2. Simplified schematic of the wideband LNA.

In order to optimize the power consumption performance and noise performance, the number of the stages of the amplifier and the bias current are determined carefully. To make sure the transistor operates in the linear region, the drain bias

voltage of the transistor is at least 1.0 V. Hence with fixed 3 V battery supply, we have three scenarios; a 1) one-stage amplifier design with the drain bias at 3.0 V, 2) two-stage amplifier design with current sharing bias topology and drain bias voltage of each transistor at 1.5 V as shown in Fig. 1, and 3) a three-stage design, which is similar with Fig. 1 except that we add one more stage into the design and end up with the drain of each transistor biased at 1.0 V. We assume perfect inter-stage matching between two transistors and plot the gain and NF performance versus power consumption of the three different scenarios at 10.6 GHz, the highest end frequency of the UWB band

D. Forward Combining Technique

The idea of forward combining technique is illustrated in Fig. 1. The RF signals at the drain node and source node of the transistor are in anti-phase because they are derived from common-source and common-drain amplifications, respectively. The signal at drain node is shifted to have 90 phase advance and the signal at source node is shifted to have 90 phase lag. These two phase-shifted signals, which are in phase, are combined together before going into the next stage circuit .Since the two signals are in phase, the overall amplifier gain is boosted. The 90 phase shifts can simply be realized by an inductor and a capacitor. Fig. 2 shows the vector diagram of the signals. The noise figure of the amplifier can also be reduced through the gain enhancement because the noise resistance Rn is inversely proportional to the square of the trans conductance's
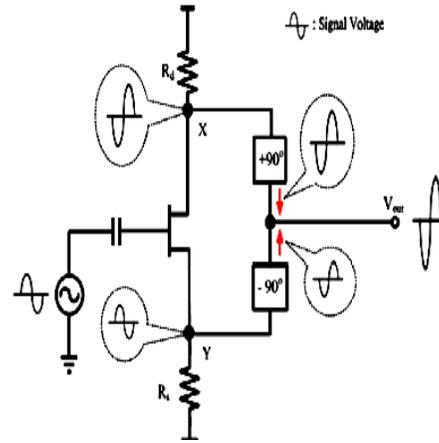

Fig. 3 Illustration of forward combining technique.

$$R_n = \frac{\gamma g_{d0}}{g_m^2}$$

E. Gate-Inductive Gain-Peaking Technique

In this technique, only the first and second cascode amplifier stages utilize the gate-inductive gain-peaking scheme for the enhancement of maximum available gain. The last stage is in a conventional cascode structure to maintain a good isolation between the RF input and output ports, Since the gain-peaking inductor degrades the port-to-port

isolation, it is worth noting the cascade effect between the first and second cascode amplifier stages. In this work, the gate inductor is tuned after the first stage design.
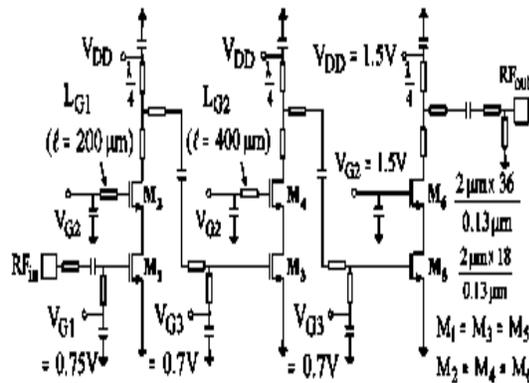

Fig. 5. Schematic of the low-power, high-gain V-band LNA.