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VLSI DESIGN AND IMPLEMENTATION OF FIR DIGITAL FILTER USING LOW POWER MAC

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ABSTRACT

In the majority of digital signal processing (DSP) applications the critical operations are the multiplication and accumulation. Multiplier-Accumulator (MAC) unit that consumes low power is always a key to achieve a high performance digital signal processing system. Finite impulse response (FIR) filters are widely used in various DSP applications .The purpose of this work is to design and implementation of Finite impulse response (FIR) filter using a low power MAC unit with clock gating and pipelining techniques to save power.

KEYWORDS - MAC, Low Power, Glitch Reduction, Clock Gating, Latch Based Design, Pipelining.

1. INTRODUCTION

Finite impulse response (FIR) filters are widely used in various DSP applications .This paper describes an approach to the implementation of low power digital FIR filter based on field programmable gate arrays (FPGAs).The advantages of the FPGA approach to digital filter implementation include higher sampling rates than are available from traditional DSP chips, lower costs than an ASIC for moderate volume applications, and more flexibility than the alternate approaches. Firstly, a single MAC unit is designed, with appropriate geometries that give optimized power, area and delay. Similarly, the N no. of MAC units are designed and controlled for low power using a control logic that enables the each stage at appropriate time. Multiply –Accumulator unit has become one of the essential building blocks in digital signal processing applications such as

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digital filtering, speech processing, video coding and cellular phone.

2. MULTIPLY-ACCUMULATE UNITS

A variety of approaches to the implementation of the multiplication and addition portions of the MAC function are possible. A conventional MAC unit consists of multiplier and an accumulator that contains the sum of the previous consecutive products. The structure of MAC unit is illustrated in Fig.1. It consists of multiplying 2 values, then adding the result to the previously accumulated value, which must then be restored in the registers for future accumulations. The function of the MAC unit is given by the following equation:

$$F = \sum_{i=0}^{N-1} a_i b_i$$

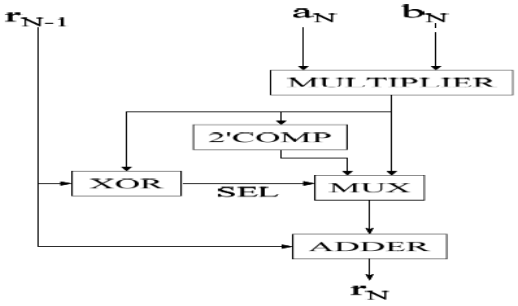

Figure 1: Clock gating Implementation

3. FIR FILTERS

The output of a FIR filter is described by the following equation:

$$y[n] = a_0 x[n] + a_1 x[n-1] + ... + a_{N-1} x[n-N]$$

x[n] is the input signal. y[n] is the output signal. a_i are the filter coefficients, also known as tap weights, that make up the impulse response. The output y of a FIR system is determined by convolving its input signal x with its impulse response a.

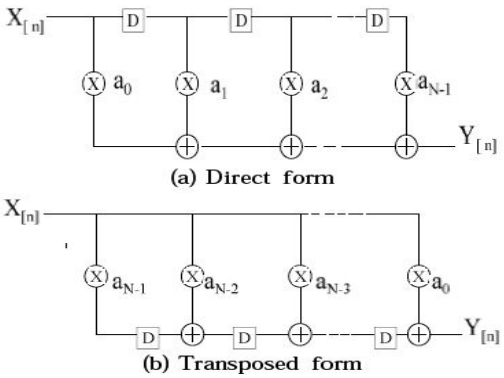

Figure 2: Various Realizations of FIR Filters

In general, there are two popular forms to realize FIR filters: direct and transposed shown in Fig. 2. In the direct form, there are delay units between multipliers. At a time, the present filter input, x(n), and N-1 previous samples of the input are fed to each multiplier input, and the filter output y(n) is the sum of product of every multiplier. In the transposed form, however, delay units are placed between adders so that the multipliers can be fed simultaneously. For the computation of FIR filter, we have to convolve the input data with filter coefficient; convolution

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process contains number of multiplication and addition.

4. LOW-POWER DESIGNS

Design for low power has become increasingly important in a wide variety of applications, including digital signal processing, mobile computing, high performance computing, and high-speed networking. This section describes various low-power design techniques that can be applied to current FPGA technology. In CMOS circuits, the dominant source of power dissipation is the dynamic power dissipation which is due to the switching of CMOS gates. This includes the clock distribution network consumption and the parasitic power due to glitches.

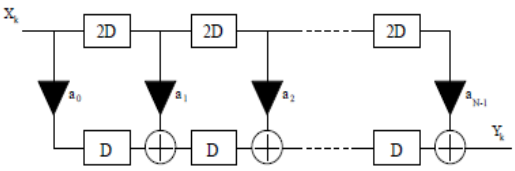

Figure 3: Direct pipe line form of N-tap FIR Filter

4.1 GLITCH REDUCTION

For arithmetic circuits, a large portion of the dynamic power is wasted on un-productive signal glitches. Glitches are due to converging combinatorial paths with different propagation delays. Signal glitching refers to the transitory switching activity within a circuit as logic values propagate through multiple levels of combinational logic.

4.1.1. Pipelining

Pipelining is a simple and effective way of reducing glitching, and hence minimizing power consumption. It is found that, at a given clock speed, pipelining can reduce the amount of energy per operation by between 40% and90% for applications such as integer multiplication, CORDIC, triple DES, and FIR filters.

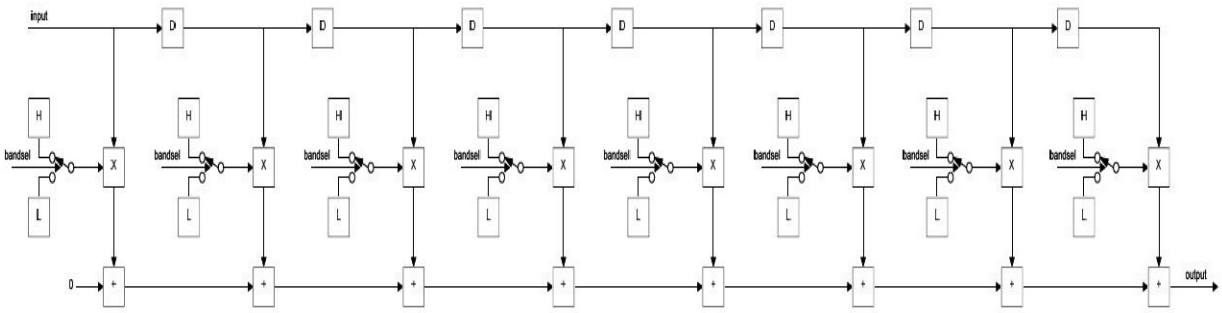

Figure 4: Basic structure of 8 tap FIR filter

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5. 8 TAP FIR FILTERS

In this paper we propose a design of 8 tap FIR filter as shown in fig 3. From this figure 3 the input is delayed and given to multiplier each multiplier gives products corresponding to different filter coefficients and all these products are accumulated and give FIR filter output. We used H and L coefficient from DB3 filter from mat lab and suitably convert these values into binary for input to design filter else we can give any coefficient to this filter.

6. DYNAMIC POWER DISSIPATION

Dynamic power makes up a large portion of the total amount of power consumed by an FPGA design. In CMOS circuits, the dominant source of power dissipation is the dynamic power dissipation. Whenever the logic level changes at different points in the circuit because of the change in the input signals the dynamic power dissipation occurs. Dynamic power is determined by the following equation.

$$P_D = \alpha C V^2 f$$

Where alpha is the switching activity factor, C is the capacitance, V is the supply voltage, and f is the clock frequency. In addition to voltage and physical capacitance, switching activity also influences dynamic power consumption. A chip may contain an enormous amount of physical capacitance, but if there is no switching in the circuit, then no dynamic power will be consumed. The data activity determines how often this switching occurs.

7. CLOCK GATING OF LATCH BASED DESIGN

In some applications, latch-based designs are preferred to D Flip Flop (DFF)–based designs. The basic concept is that a DFF can be split into two latches, and each one is clocked with an independent clock signal.

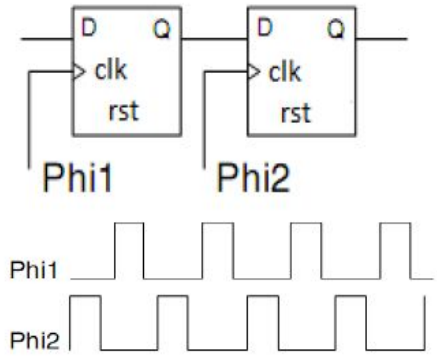

Figure 5: Clock gating of latch-based design

8. RESULTS AND DISCUSSION

In this chapter, the 8_Tap FIR filters are implemented on FPGA using MAC. The filter specifications are real world and

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windowing method is used to design the filter coefficients. These coefficients are used to implement filter on Xilinx FPGA Spartan 3E kit using Xilinx ISE 14.6i. Here we are using two methods to implement the filter on FPGA.

TABLE I

POWER ANALYZER SUMMARY	
8 tap FIR filter	**Core dynamic thermal power dissipation**
Original Filter	21.40mW
Latch Base Filter	1.73mW
Pipelined Filter	1.09mW
MAC Unit	0.007698m W

9. 8_TAP FIR FILTER

A FIR filter scheme suitable for unsigned and signed computations is presented in this paper. Low power designs for 8 Tap FIR filter using latch based and pipelining techniques are implemented. These filters are designed using XILINX and developed VERILOG code. Simulation is performed using Active-HDL and functional verification is carried out using SPARTAN 3E and, FPGA implementation on Cyclone. Figure shows below simulation result performed in Active-HDL for 8 tap FIR filter. Simulation result of FIR filter is shown in figure below

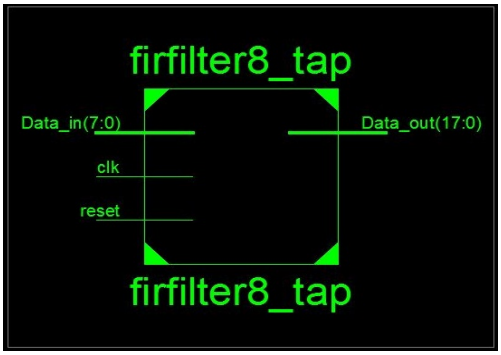

Figure 6: Block diagram of the 8 Tap FIR Filter

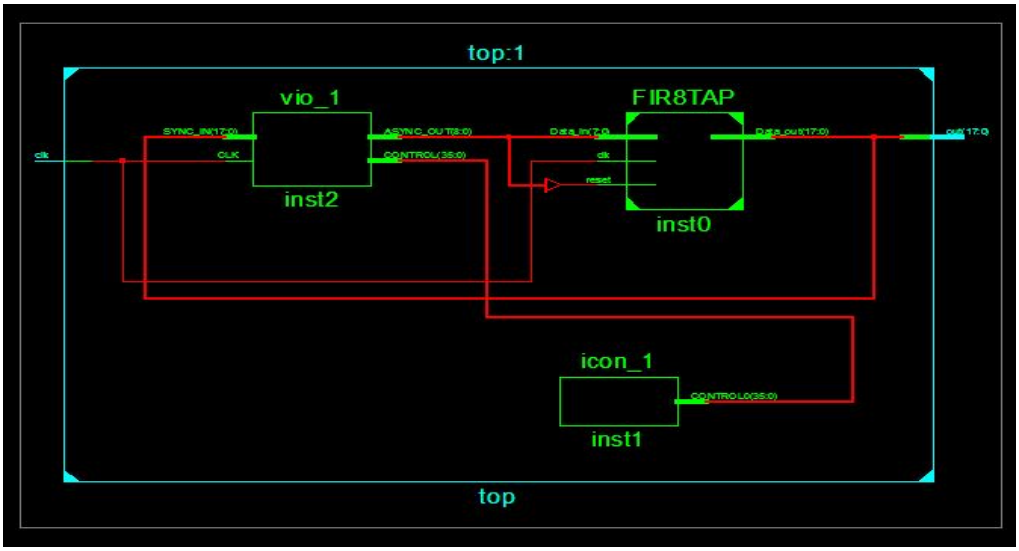

Figure 7: RTL Schematic view of 8 tap FIR filter

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Figure 8: RTL Schematic view of 8 tap FIR filter

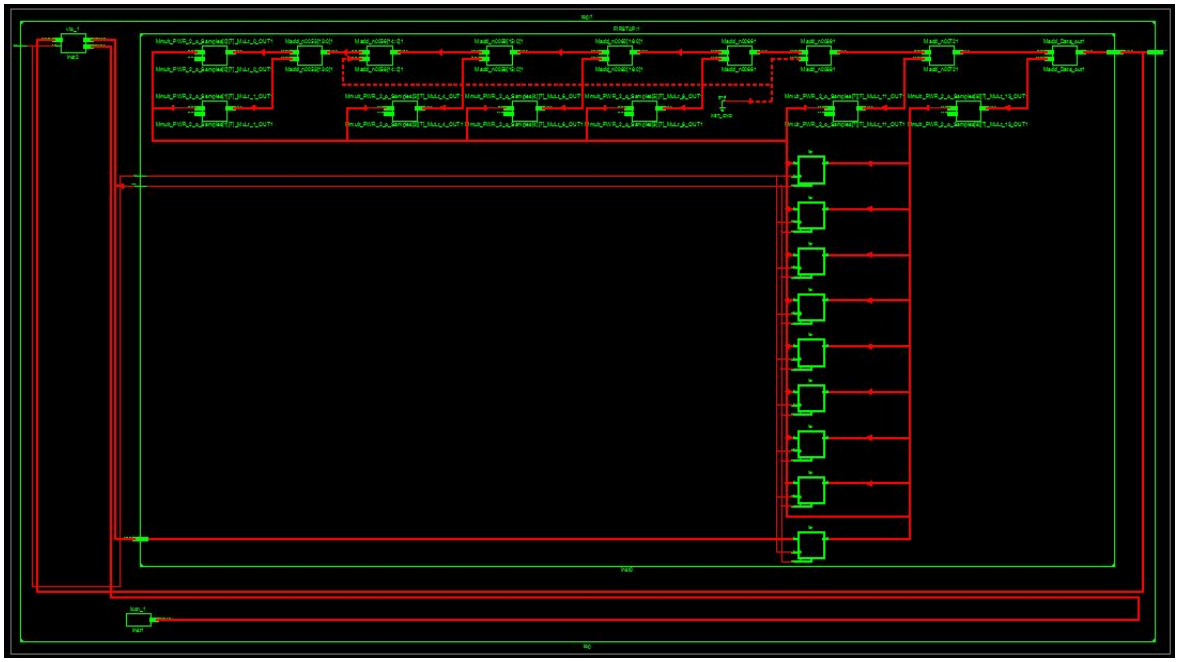

Figure 9: Technology Schematic view of 8 tap FIR filter

Now the generated circuit is simulated using Xilinx simulator with certain inputs and output waveform are shown in Figure 10.

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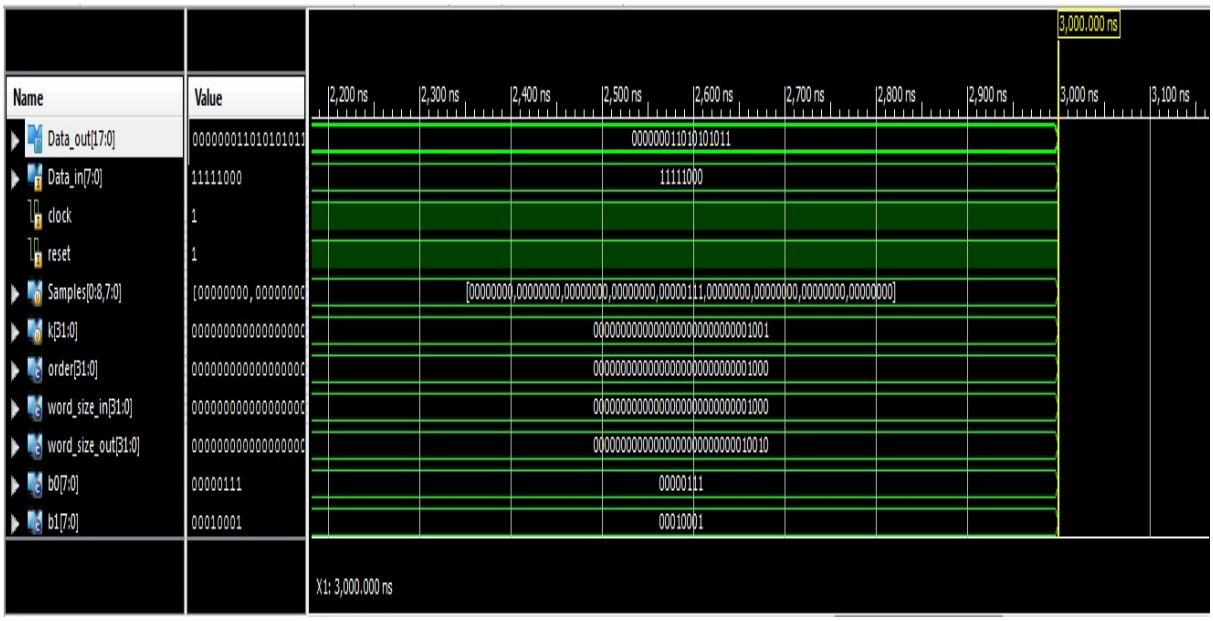

Figure 10: Input and Output waveform of Simulation

10. CONCLUSION

Design for low power 6 tap FIR filter has been presented in this paper. The power reduction is achieved through the usage of a MAC unit inside the filters that reduce the total activity and therefore the dynamic power. The basic building blocks for the MAC unit are identified and each of the blocks is analyzed for its performance. Power is calculated for the blocks. 1-bit MAC unit will be designed with enable to reduce the total power consumption based on above proposed techniques. Active-HDL together with Altera Quartus II tool is used effectively to model dynamic transient signal activity and produce accurate power consumption estimation. It is seen by above results that Latch based design can reduce the dynamic power consumption by 92% and pipelining reduces that up to 95%.

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