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Analysis of Leakage Reduction Technique on Different SRAM Cells

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Abstract **: Leakage components is very important for estimation and reduction of leakage power, especially for low power applications. This provides the motivation to explore the design of low leakage SRAM cells. High leakage currents in deep submicron regimes are becoming a major contributor to total power dissipation of CMOS circuits as the threshold voltage, channel length and gate oxide thickness are scaled. Memory leakage suppression is critically important for the success of power-efficient designs, especially for ultra- low power applications. As the channel length of the MOSFET reduces, the leakage current in the SRAM increases. One method is to reduce the standby supply voltage (VDD) to its limit, which is the Data retention voltage (DRV), leakage power can be substantially reduced. Also, lower operating voltage will lower the stability of SRAM cell resulting in lower value of static noise margin. To reduce the sub-threshold leakage further, an adaptive voltage level (AVL) circuit is added to this cell, which controls the effective voltage across the SRAM cell in inactive mode. Two schemes are employed; one in which the supply voltage is reduced and the other in which the ground potential is increased. CADENCE Simulations are performed with 90nm CMOS technology process file and the leakage currents of all the cells are measured and compared. Simulation results revealed that there is a significant reduction in leakage current for this proposed cell with the AVL circuit reducing the supply voltage.**

Key words: **Leakage power, SRAM, leakage reduction techniques**

I. INTRODUCTION

As technology scales down, the supply voltage must be reduced such that dynamic power can be kept at reasonable levels and power delivery can still be performed within the functional requirements. However, as a result of scaling, power dissipation due to leakage currents has also increased dramatically and is a major source of concern especially for low power applications. This paper introduces how to control the leakage current in SRAM cell and optimizes the power. The amount of embedded SRAM in modern micro-processors and systems-on-chips (SOCs) increases to meet the performance requirements in each new technology generation [1].

Till now the dominant leakage mechanism has been due to drain source sub-threshold current. With scaling of channel length, oxide thickness also needs to be scaled to maintain proper operation of MOS transistor. Assuming this leakage mechanism, a number of techniques have been proposed in literature for reducing the impact of leakage power dissipation such as gated-VDD scheme [2], Dual-Vth SRAM [3] etc. With scaling of channel length, oxide thickness also needs to be scaled to maintain new generations of technology, the magnitude of gate leakage current has increased steadily and is likely to become comparable or even larger than the sub-threshold leakage for future CMOS devices [4]. Of the several techniques which have been proposed to reduce sub-threshold leakage in SRAM cells [3], [1], [2], use of a self-controllable switch (SVL) [5] which allows full supply voltage to be applied in active mode and reduced supply voltage in inactive mode appears to be particularly promising for reducing gate leakage currents as well. An SVL can be used either to reduce the supply voltage to the SRAM cell or increase the potential of ground node and the two approaches can be combined as well. Although a technique similar to use of SVL for raising the ground potential has already been reported to yield significant reduction in gate leakage currents [5]. So, in this work, in order to suppress the leakage further, the proposed SA cell combined with adaptive voltage level (AVL) circuit either at the ground node (referred as AVLG) or the supply node (referred as AVLS) is simulated and its leakage characteristics are analysed.

The paper is organized as follows. Section 2 describes the conventional 7T SRAM cell and 8T SRAM Cell and its working. Section 3 describes the AVLG circuit in 7T SRAM cell and 8T SRAM cell and its effect on leakage reduction. Section 4 describes the AVLS circuit in 7T SRAM cell and 8T SRAM cell and its effect on leakage reduction. Section 5 gives the simulation results and discussion. Section 6 gives the conclusion.

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II. WORKING OF 7T & 8T SRAM CELLS

A. 7T SRAM CELL

As the name suggests the cell consist of 7 transistor-2 PMOS and 5 NMOS. Two inverters are designed and are connected as a cross coupled known as active transistor. There are two transistors which are known as pass transistors. Pass transistors are connected to the bit lines (BL and BLB).There are two word lines which are used for read and write operation. The read and write operations are controlled by the last transistor which is the most important transistor for the whole circuit operation. Fig. 1 shows the schematic of 7T SRAM cell.

The write operation depends on cutting off the feedback connection between the two inverters, invl and inv2, before the write operation and then again making the feedback connection for the read Operation. The feedback connection and disconnection are performed through the transistor N5.The cell only depends on BLB to perform a write operation. The BLB and the pass transistor N3 are used for transferring new data into the cell. Alternatively, the BL and the transistor stack formed by N4 and N5 are used for reading data from the cell. Two separate control signals RL and WL are used for controlling the read and the write operations, respectively. The write operation starts by turning N5 off to cut off the feedback connection. BLB carries complement of the input data. During the write operation N3 is turned on, and N4 is kept off. The BL_bar transfers the complement of input data to inv2 to develop Q, cell data, which drives invl and develops QB. When writing "0", BLB is kept "high" with negligible write power consumption. To write "1", BL_bar is discharged to "0" with comparable power consumption to a conventional write.

During read operation, the cell behaves like a conventional 6T SRAM cell and N5 is kept on. When Q= "0", the read path consists ofN2 and N4, and exactly behaves like the conventional cell. When Q= "1", the read path consists of N1, N5 and N3 that represents a critical read path .The sense amplifier is used for the read operation to get the output by sensing and amplifying the BL and BLB.

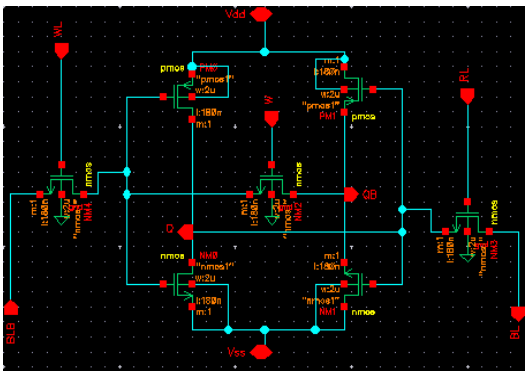

Fig .1. Schematic of 7T SRAM cell

B. 8T SRAM CELL

Figure 2 shows the architecture of new 8T SRAM cell. It consists of two extra transistors MNLL and MNWL as compared to conventional 6T SRAM cell. Transistor MNLL is used to reduce gate leakage while transistor MNWL is used to make cell SNM free in the zero state. Interestingly, transistor MNLL also helps in improving SNM when cell holds logic '1'. The signal WLB is the complement of word line (WL) signal.. 8T transistor consist of 8 transistor-2 PMOS and 6 NMOS. In this work, the basic read/write operations of 8T SRAM cell are performed using single ended sense amplifier.

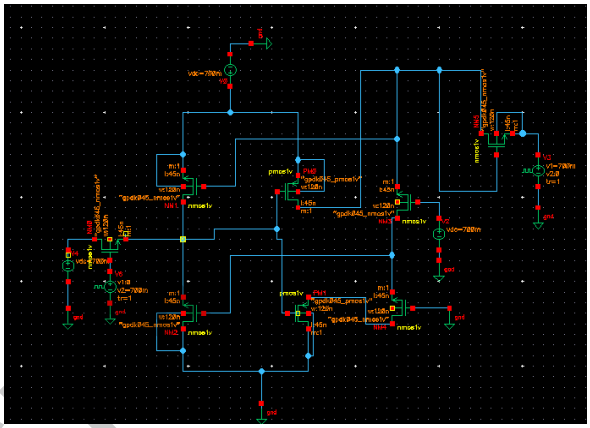

Fig .2. Schematic of 8T SRAM cell

In write '0' operation, the bit-line BT is pulled down to logic '0'.As soon as the signal WL rises from logic '0'to logic '1', transistor MNWL is turned off. The node XT starts discharging which turns on bit-line BB is pulled down to-VTN, where VTN is the threshold voltage of transistor MN4. The node XB starts discharging which turns on transistor MP1. Once transistor MP1 is turned on, the node XT is at logic '1' and hence logic '1' is written into the cell. In read operation, the bit-lines BT and BB are held at logic '1' by the pre-charged circuitry. In read'0' operation, the bit-line BT starts discharging through transistors MN3 and MN1. The single ended sense amplifier [4] gives output as logic '0' when bit-line BT falls below a certain threshold voltage (decided by single ended sense amplifier design) from logic '1'. In read '1' operation, the bit-line BT remains at logic '1' because storage node XT is at logic '1' and hence single ended sense amplifier output remains at logic '1'.

During read '1' operation, transistors MNWL and MP2 are turned off. For this scenario, the retention time for holding logic '0' at node XB is calculated given by equation t=C.dV/I, Where C is the total capacitance at node XB, dV is the threshold voltage of transistor MN1 and I is the leakage current through transistor MP2 respectively.

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In standby mode, where the cell is in zero state, the transistor MNLL enters cut-off as its source voltage is at VDD-VT, resulting in reduced direct tunnelling leakage through transistor MN1. The voltage at the storage node is not affected by the design in zero state. However, the trans-conductance of transistor MN1 has been reduced which may affect the performance of the cell as discussed in section simulation results. When cell is holding logic '1' in the standby mode, the transistor MNLL serves as a good conductor of logic'0'[5]. Since transistor MNWL is on in standby mode, for this case the functioning of cell is same as the conventional 6T SRAM cell except transistor MNWL and MNLL. In this case where cell holds logic '1', both the transistors MNLL and MNWL are the extra sources of direct tunneling leakage.

III. LEAKAGE CONTROL USING AVLG in 45nm

A. 7T SRAM and 8T SRAM

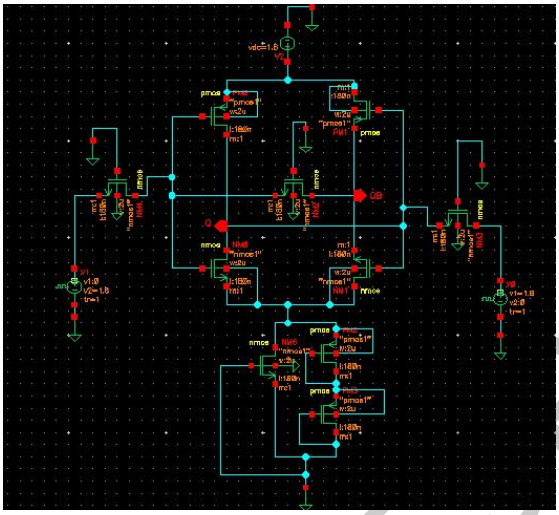

Fig.3. Schematic of 7T SRAM cell using AVLG technique

Fig.3 shows a schematic of an 7T SRAM cell in which AVLG scheme is applied. The switch provides 0 Volt at the ground node during the active mode and a raised ground level (virtual ground) during the inactive mode. This scheme is similar to the diode footed cache design scheme proposed to control gate and sub-threshold leakages in SRAM, in which a diode designed with high Vt MOS transistors was used to raise the ground level of SRAM in the inactive mode [5].

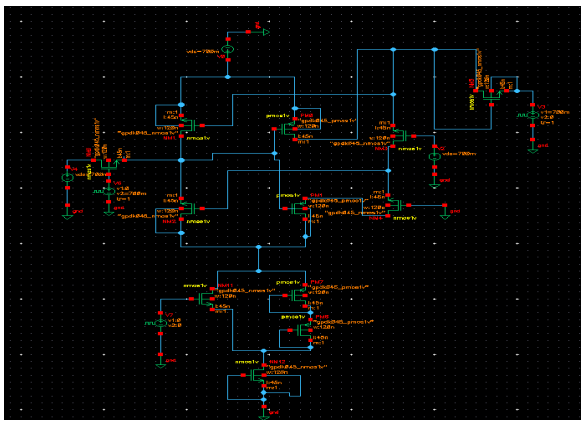

Fig.4. Schematic of 8T SRAM cell using AVLG technique

Fig. 4 represents the schematic of 8T SRAM cell using AVLG technique. The switch provides 0 Volt at the ground node during the active mode and a raised ground level (virtual ground) during the inactive mode. An increase in virtual ground voltage reduces the gate-source and gate-drain voltage of transistor M1 and also the gate drain voltage of transistor M2, which results in a sharp reduction in gate leakage currents of these two transistors. There is no improvement in gate leakage currents of transistors M5 and M6. But an additional gate leakage appears in transistor M5 due to increase in drain voltage of M1. Incorporation of SVL results in another new gate leakage current through NMOS transistor NL1 in the AVLG switch. Although only one transistor is normally used for one bank of SRAM cells, leakage current through it is not necessarily negligible because its size has to be much larger than NMOS transistors within the SRAM cell to avoid performance degradation in the active state. As far as sub-threshold leakage currents are concerned, AVLG approach is successful in reducing currents through M3, M2 and M5 as well. To summarize, all sub-threshold currents are reduced using AVLG approach, it is only partially successful in reducing gate leakage currents.

IV. LEAKAGE CURRENT USING AVLS

A. 7T and 8T SRAM CELL

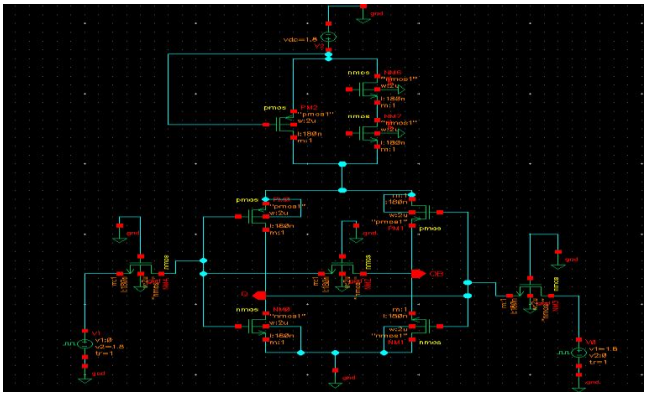

Fig.5. Schematic of 7T SRAM cell using AVLS technique

An 7T SRAM cell incorporating AVLS scheme is shown in Figure 5. In this scheme, a full supply voltage of VDD is applied to SRAM in active mode while a reduced supply voltage of VD is applied in inactive mode.

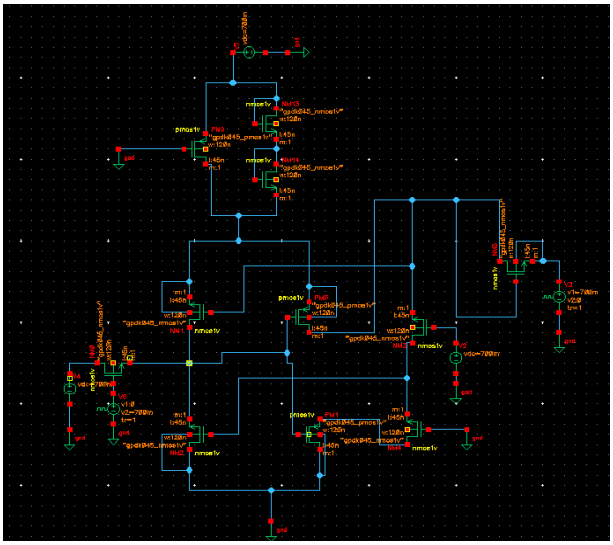

Fig.6. Schematic of 8T SRAM cell using AVLS technique

An 8T SRAM cell incorporating AVLS scheme is shown in Figure 6. In this scheme, a full supply voltage of VDD is applied to SRAM in active mode while a reduced supply voltage of VD is applied in inactive mode.
Since transistor M4 is in ON state, the drain voltages of transistors M2 and M1 are also at VD. As a result of a decrease in gate voltage of transistor M1, gate leakage current through it is sharply reduced. A decrease in drain voltage of transistor M2 results in lower gate-drain voltage across it and thus gate leakage current through it is also reduced. The gate leakage through transistor M5 remains unchanged. As far as the subthreshold leakage currents are concerned, they are reduced in transistors M2 and M3 but remain unaltered in M3. A decrease in source voltage of M6 results in a decrease in one component of EDT leakage across it while leaving the other unchanged. Gate leakage across transistor M5 remains unchanged. Transistor PU1 being a PMOS transistor does not result in any significant added leakage current as a result of transistors used in AVLS circuit. One thus sees that AVLS scheme has a better impact on gate leakage current reduction than the AVLG scheme. To summarize, the AVLS approach, while more successful in reducing gate leakage current, still leaves two gate leakage current components in access transistors unaltered. It also leaves one sub-threshold current component in access transistor unchanged and results in an additional sub-threshold leakage current across the other access transistor.

V. SIMULATION RESULT

The leakage currents in the conventional and the schemes suggested in this section. Simulation results are simulated on the 45nm CADENCE tool with a nominal supply voltage 0.7 volt. The gate leakage being the only dominant mechanism at room temperature, AVLG scheme suppresses the total leakage of 7T by 14%, while AVLS scheme without changing bit-line voltages provides a leakage reduction of 21% Where as total leakage of 8T reduces by 13% in AVLG scheme, while AVLS scheme without changing bit-line voltages provides a leakage reduction of 37%.

TABLE I: Leakage current of 7T SRAM in 45nm

Reduction Scheme	Voltage	Leakage current
7T SRAM cell	0.7 v	2.17696 PA
AVLG	0.7 v	1.91583 PA
AVLS	0.7 v	1.88323 PA

TABLE II: Leakage current of 8T SRAM in 45nm

Reduction Scheme	Voltage	Leakage current
8T SRAM cell	0.7 v	3.4186 PA
AVLG	0.7 v	2.9798 PA
AVLS	0.7 v	2.1543 PA

The output waveform of 7T and 8T SRAM cell waveform are given in Fig.7 and Fig. 8.

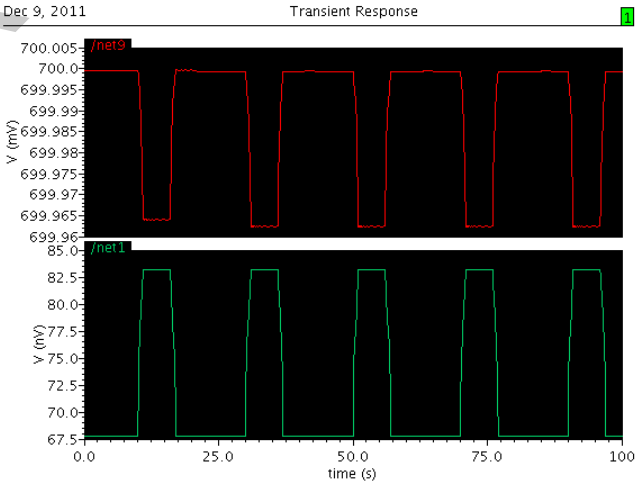

Fig. 7. Output waveform of 7T SRAM cell

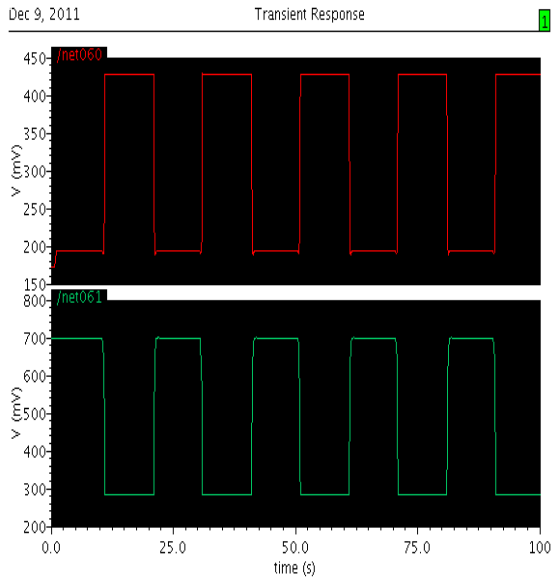

Fig. 8. Output waveform of 8T SRAM cell

The Leakage current waveform of 7T and 8T SRAM cell using AVLG technique is given in fig. 9 and fig.10.

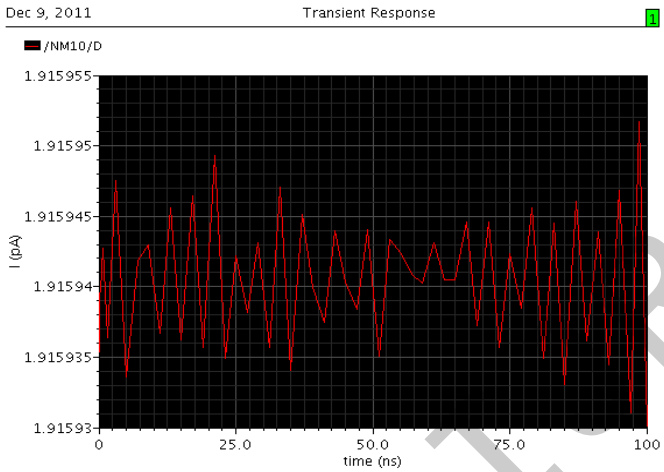

Fig. 9 Leakage current in 7T SRAM cell using AVLG technique.

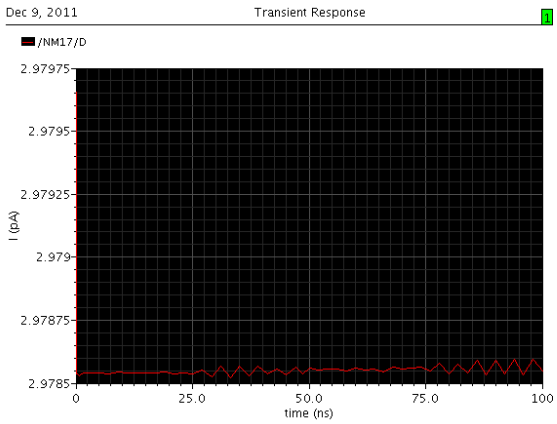

Fig. 10 Leakage current in 8T SRAM cell using AVLG technique.

The Leakage current waveform of 7T and 8T SRAM cell using AVLS technique is given in fig. 11 and fig.12.

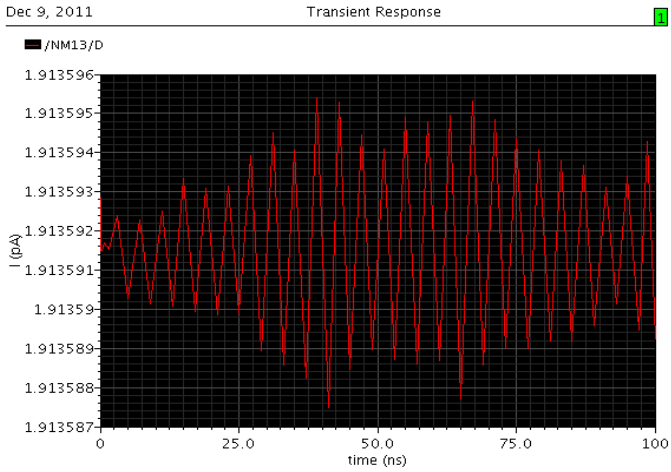

Fig. 11 Leakage current in 7T SRAM cell using AVLS technique.

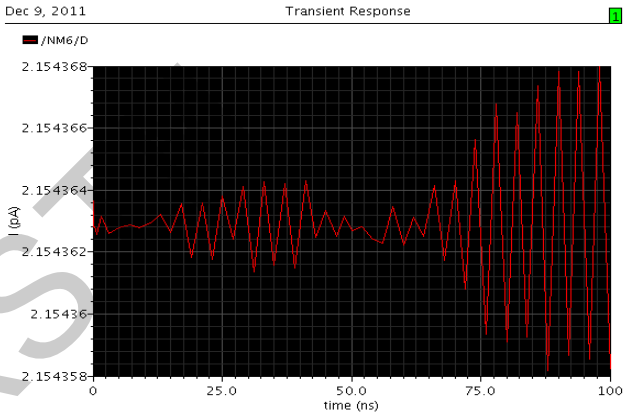

Fig. 12 Leakage current in 8T SRAM cell using AVLS technique.

VI. CONCLUSION

A novel asymmetric SRAM cell (SA cell) was proposed that offers reduced gate and sub threshold leakage currents in caches. The novel SRAM design exploits the fact that most of the bits stored in caches are zeroes. Simulation results show that 61% reduction in the total leakage currents was achieved at 27°C with marginal degradation in the performance compared to the conventional 8T cell. Two schemes: a) raising the ground level and b) decreasing the supply voltage to the SRAM cell during inactive mode to suppress its leakage currents were also examined in detail. It was observed that the scheme using supply voltage reduction is more efficient than the one raising the ground potential. It was found that while the LSVL approach is better in terms of reduction in sub-threshold leakage current, the USVL approach performs better with respect to gate leakage currents.

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