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OVERVIEW: NETWORK ON CHIP-3D ARCHITECTURE

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ABSTRACT

As the feature size in deep-submicron domain is continuously shrinking and the bandwidth requirements is increasing, traditional shared-bus architecture will no longer be able to meet the requirements of System-on-Chip (SoC) implementations. Specially, inherently non-scalable nature of the shared-bus architecture as well as its power hungry nature will become the communication bottleneck in most practical applications. Network-on-Chip(NoC) communication architectures have emerged as a promising alternative to address the problems associated with on-chip buses by employing a packet-based micro-network for inter-IP communication. The semiconductor industry is now moving towards the 3D stacking technology for the forthcoming nano scale generation with the advancement in transistor packing density. The greatest advantage for 3D NoC is that it can greatly help in reducing the diameter of the topology of NoC leading to reduction in packet transfer time and latency.

KEYWORDS: Network on Chip, 2D & 3D Mesh architecture.

I. INTRODUCTION

Imagine a situation where you need to travel between your home and office every day. You need to put up with time lost during commute as well as paying for the fuel. One possible solution is to have your home in another floor of your office building. In this way, all you need to do is to go up and down between floors and you can save time and cost. This simple idea can similarly be applied to boost the overall performance in future integrated circuits [2].

For the past 40 over years, higher computing power was achieved primarily through commensurate performance enhancement of transistors as a result of continuously scaling down the device dimensions in a harmonious manner. This has resulted in a steady doubling of device density from one technology node to another as famously described by Moore's Law. Improvement in transistor switching speed and count are two of

The most direct contributors to the historical performance growth in integrated circuits (particularly in silicon-based digital CMOS).This scaling approach has been so effective in many aspects (performance and cost) that integrated circuits have essentially remained a planar platform throughout this period of rigorous scaling. As performance enhancement through geometrical scaling becomes more challenging and demand for higher functionality increases, there is tremendous interest and potential to explore the third dimension, i.e., the vertical dimension of the integrated circuits.

Three-dimensional integrated circuits (3D IC) refers to a stack consists of multiple ultra-thin layers of IC that are vertically bonded and interconnected with through Silicon via (TSV) as shown in Figure-1. In 3D implementation, each block can be fabricated and optimized using their respective technologies and assembled form a vertical stack. 3D stacking of ultra-thin ICs is identified as an inevitable solution for future performance enhancement, system miniaturization, and functional diversification.

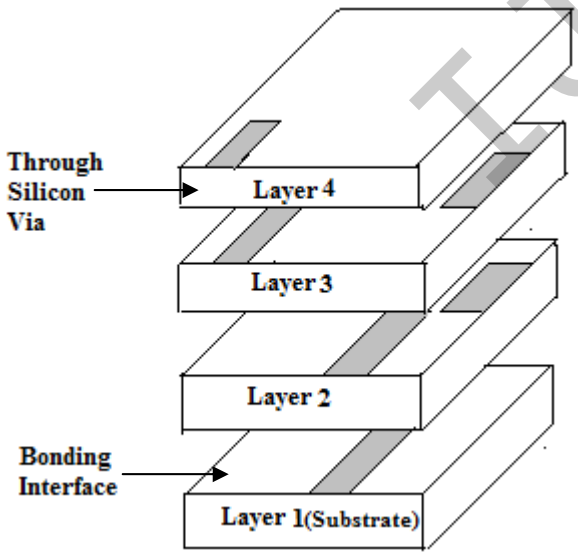


Figure-1: Representation of 3D IC

2. 3D NoC ARCHITECTURE

Enabling design in the vertical dimension permits a large degree of freedom in choosing an on-chip network topology. Due to wire-length constraints and layout complications, the more conventional two-dimensional integrated circuits have placed limitations on the types of network structures that are possible. With the advent of 3D ICs, a wide range of on-chip network structures that were not explored earlier are being considered [1][3].

One of the well-known 2D NoC architectures is the 2D Mesh as shown in Figure-2.This architecture consists of an $m \times n$ mesh of switches interconnecting IP blocks placed along with them. It is known for its regular structure and short inter-switch wires. From this structure, a variety of three-dimensional topologies can be derived. The straightforward extension of this popular planar structure is the 3D Mesh. Figure-3.Shows an example of 3D Mesh NoC. It employs 7-port switches: one port to the IP block, one each to switches above and below, and one in each cardinal direction.

A second derivation, 3D Stacked Mesh as shown in Figure-4, takes advantage of the short inter-layer distances that are characteristics of a 3D IC, which can be around 20μm[4].The 3D Stacked Mesh architecture is a hybrid between a packet-switched network and a bus. It integrates multiple layers of 2D Mesh networks by connecting them with a bus spanning the entire vertical distance of the chip. As the distance between the individual 2D layers in 3D IC is extremely small, the overall length of the bus is also small, making it a suitable choice for communicating in the z-dimension. Furthermore, each bus has only a small number of nodes, keeping the overall capacitance on the bus small and

greatly simplifying bus arbitration. For consistency with, this analysis considers the use of a dynamic, time-division multiple-access bus, although any other type of bus may be used as well. A switch in a 3D Stacked Mesh network has, at most, 6 ports: one to the IP, one to the bus, and four for the cardinal directions. Additionally, it is possible to utilize ultra wide buses similar to the approach introduced in to implement cost-effective, high-bandwidth communication between layers[5]. A third method of constructing a 3D NoC is by adding layers of functional IP blocks and restricting the switches to one layer or a small number of layers, such as in the 3D Ciliated Mesh structure. This structure is essentially a 3D Mesh network with multiple IP blocks per switch.The 3D Ciliated Mesh is a 4 × 4 × 2 3D mesh-based network with 2 IPs per switch, where the two functional IP blocks occupy, more or less, the same footprint but reside at different layers. This is shown In Figure-5.In a ciliated 3D Mesh network, each switch contains seven ports. This architecture Will clearly exhibit lower overall bandwidth than a complete 3D Mesh due to multiple IP blocks per switch and reduced connectivity. This type of network offers an advantage in terms of energy dissipation, especially In the presence of specific traffic patterns.

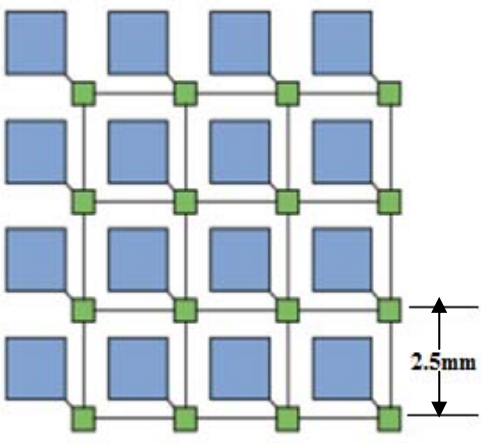


Figure-2: 2D Mesh NoC architecture

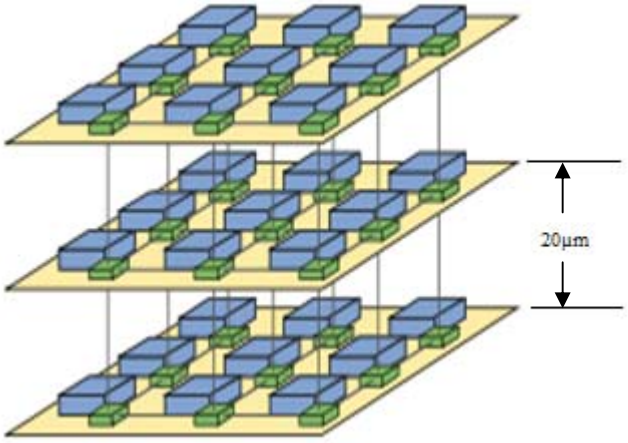


Figure-3: 3D Mesh NoC architecture

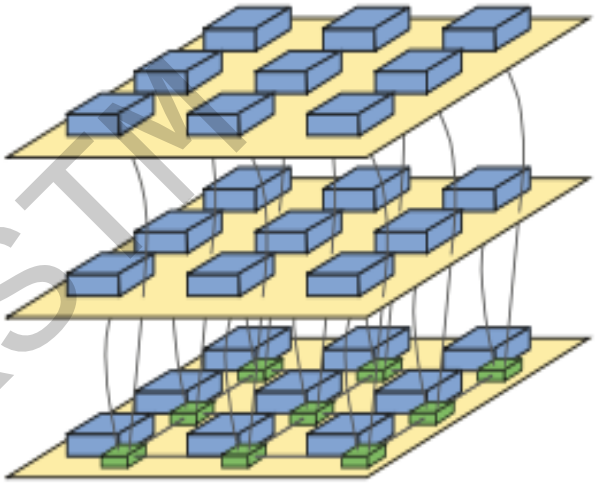


Figure-4: Stacked Mesh NoC architecture

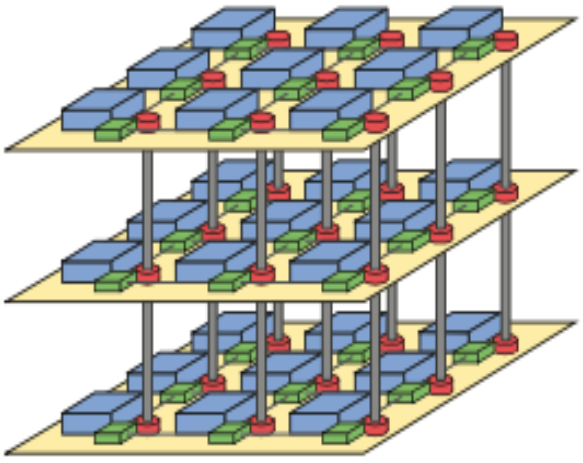
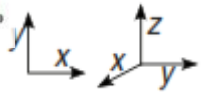


Figure-5: Ciliated 3D Mesh NoC architecture



Co-ordinate Axes

Interconnect

IP Block

Bus

Switch

Node

3. CONCLUSION

3D Network structures provide a better performance compared to traditional 2D NoC architectures. The mesh-based architectures show significant performance gains in terms of throughput, latency and energy dissipation with small area overhead.

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