MADHUR KULSHRESTHA et al.
DATE OF PUBLICATION: NOV 28, 2014

ISSN: 2348-4098
VOL 2 ISSUE 8 NOV-DEC 2014

designing of D-flip flop based on XOR/XNOR circuit because transmission gate has high switching speed, requires less power and gives less delay. Delay can be easily predicted by Spice simulations. These simulations help in minimizing chip area, power consumption, time delay and maximizing reliability. All internal capacitances are ignored. The maximum number of loading circuits that can be connected to the output of D-flip flop based on XOR/XNOR circuit is called fan-out of a circuit which helps to drive the output signal.

In this chapter I have explained and designed five CMOS structures of D-flip flop based on XOR/XNOR circuits using different design styles and compared the main factors for all the designs.

All circuits are designed using 32nm UMC CMOS technology.

Many papers are published in this area but I have designed D-flip flop using different XOR/XNOR gate circuits.

Table 1 mentions the initial parameters that are taken to make the pulse for A & B.

Table 1: Initial Parameters

V_{dd}= 0.9V, L = 32nm			
Input	Delay (sec)	Rise Time (sec)	Fall Time (sec)
A & B	0.025F	0.3P	0.3P

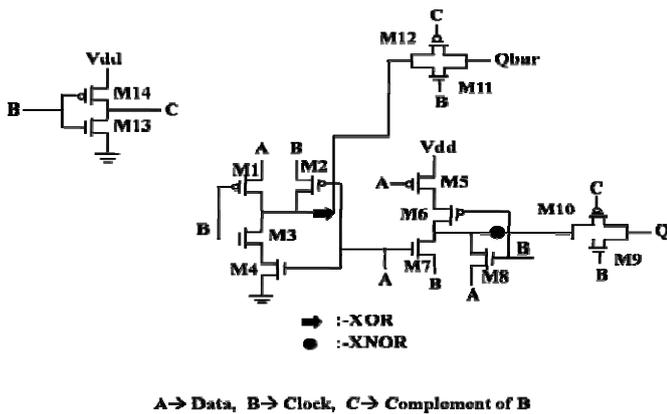## 2.1 D-Flip Flop Design-I

A→ Data, B→ Clock, C→ Complement of B

Figure 3: D-flip flop design-I

When AB=00, M1, M2, M5, M6 gets ON. At this stage M1 & M2 gives XOR output '0' and M5 & M6 gives XNOR output Vdd as '1'. Since B (Clock) is off so Q will be previous value of output. When AB=01, M2, M3, M5, M8 gets ON. At this stage M2 gives XOR output B as '1' and M8 gives XNOR output A as '0'. Since B (Clock) is high so Q will be value of A. When AB=10, M1, M4, M6, M7 gets on, at this stage M1 gives XOR output A as '1' and M7 gives XNOR output B as

'0'. When AB=11, M3, M4, M7, M8 gets on, at this stage M3 & M4 gives output '0' and M7 & M8 gives output '1'.

This is how the circuit works as a D-flip flop based on XOR/XNOR gate.

Table 2 shows the transistors characteristics at 32nm for design-I.

Table2: Transistors Characteristics for Design-I

MOSFET	W/L ratio
M1	0.438
M2	0.469
M3	0.406
M4	0.406
M5	0.406
M6	0.875
M7	0.375
M8	0.344
M9	0.344
M10	0.406
M11	0.344
M12	0.406
M13	0.344
M14	0.406
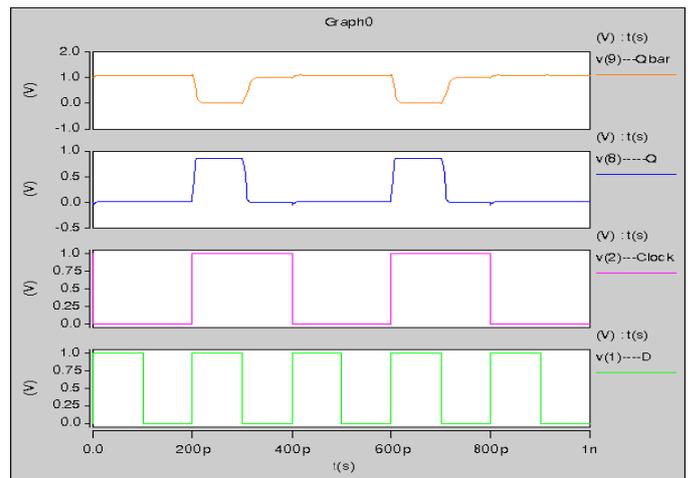
Figure 4: Output for Design-I

2.2 D-Flip Flop Design-II

A→ Data, B→ Clock, C→ Complement of B

Figure 5: D-flip flop design-II

MADHUR KULSHRESTHA et al.
DATE OF PUBLICATION: NOV 28, 2014

ISSN: 2348-4098
VOL 2 ISSUE 8 NOV-DEC 2014
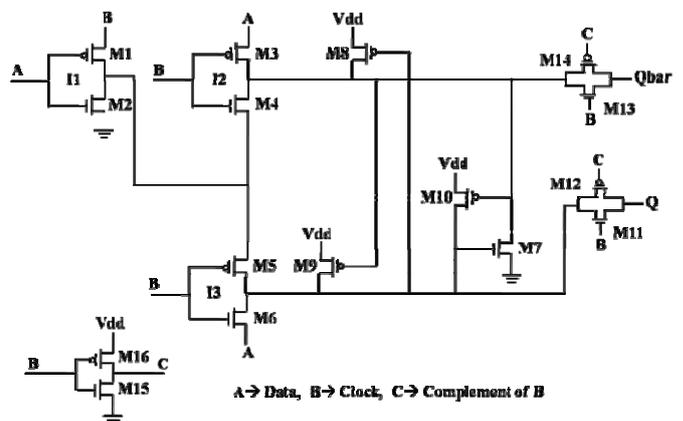
When AB=00, M1, M3, M5 gets ON. At this stage I1 produces output B and I2 produces output A. Output of I2 switches M9 & M10 on and output of M10 switches M7 on making XOR output '0' and XNOR output Vdd as '1'. Since B (Clock) is off so Q will be previous value of output. When AB=01, M1, M4, M6 gets ON. At this stage I1 & I2 produces output B and I3 produces output A making XNOR output '0'. Output of I3 switches M8making XOR output '1'. Since B (Clock) is high so Q will be value of A. When AB=10, M2, M3, M5 gets on, at this stage I1 & I3 produces output '0' making XNOR output '0'. I2 produces output A making XOR output '1'. When AB=11, M2, M4, M6 gets ON. At this stage I1& I2 produces output '0'making XOR output '0' and I3 produces output A. Output of I2 switches M9 & M10 on and output of M10 switches M7 on making XNOR output Vdd as '1'.

This is how the circuit works as a D-flip flop based on XOR/XNOR gate.

Table 3 shows the transistors characteristics at 32nm for design-II.

Table 3: Transistors Characteristics for Design-II

MOSFET	W/L ratio
M1	0.563
M2	1.094
M3	0.563
M4	1.094
M5	0.563
M6	0.344
M7	0.469
M8	0.875
M9	0.625
M10	1.000
M11	0.344
M12	0.375
M13	0.438
M14	0.438
M15	0.344
M16	0.375
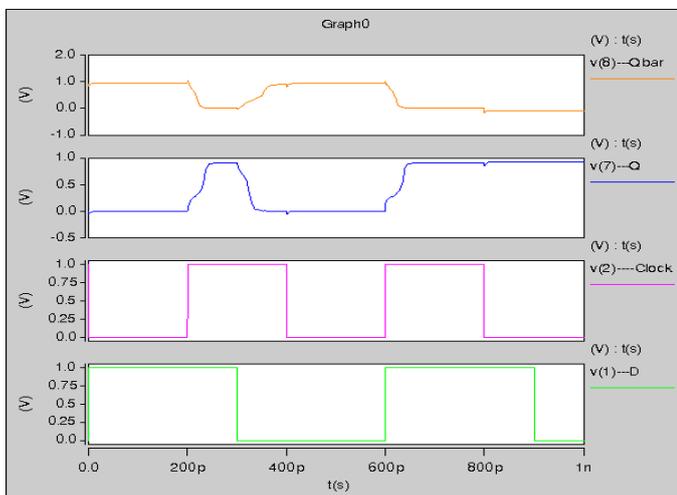
Figure 6: Output for Design-II

2.3 D-Flip Flop Design-III

A→ Data, B→ Clock, C→ Complement of B
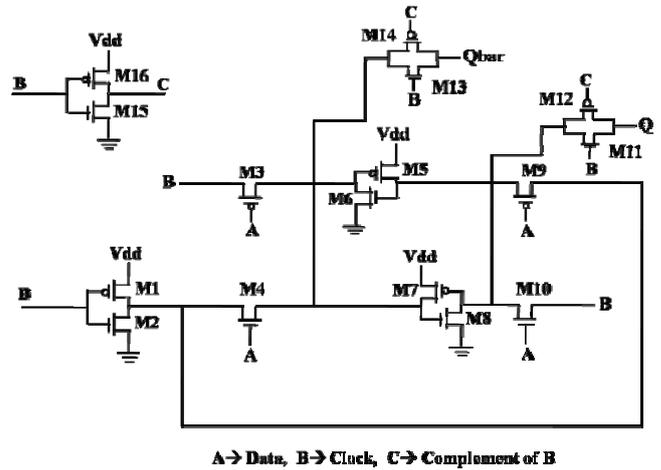
Figure 7: D-flip flop design-III

When AB=00, M1, M3, M9 gets ON. At this stage M3 produces output B (0) as an XOR output& M1 produces output '1' and provides it to M9 making XNOR output '1'. Since B (Clock) is off so Q will be previous value of output. When AB=01, M2, M3, M9 gets ON. At this stage M3 produces output B (1) as XOR output &M2 produces output '0'and provides it to M9 making XNOR output '0'. Since B (Clock) is high so Q will be the value of A. When AB=10, M1, M4, M10 gets on, at this stage M1 produces output '1' which flows through M4 making XOR output '1'. XOR output switches M8 on and produces output '0' & M10 also produces output '0' as XNOR output. When AB=11, M2, M4, M10 gets ON. At this stage M2 produces output '0' which flows through M4 and makes XOR output '0'. XOR output switches M5 on and produces output '1' & M10 also produces output '1' making XNOR output '1'.

This is how the circuit works as a D-flip flop based on XOR/XNOR gate.

Table 4 shows the transistors characteristics at 32nm for design-III.

Table 4: Transistors Characteristics for Design-III

MOSFET	W/L ratio
M1	1.094
M2	2.031
M3	1.563
M4	2.031
M5	1.250
M6	0.375
M7	0.469
M8	0.938
M9	0.375
M10	0.375
M11	0.344
M12	0.375
M13	0.375
M14	0.563
M15	0.469
M16	0.469

MADHUR KULSHRESTHA et al.
DATE OF PUBLICATION: NOV 28, 2014

ISSN: 2348-4098
VOL 2 ISSUE 8 NOV-DEC 2014

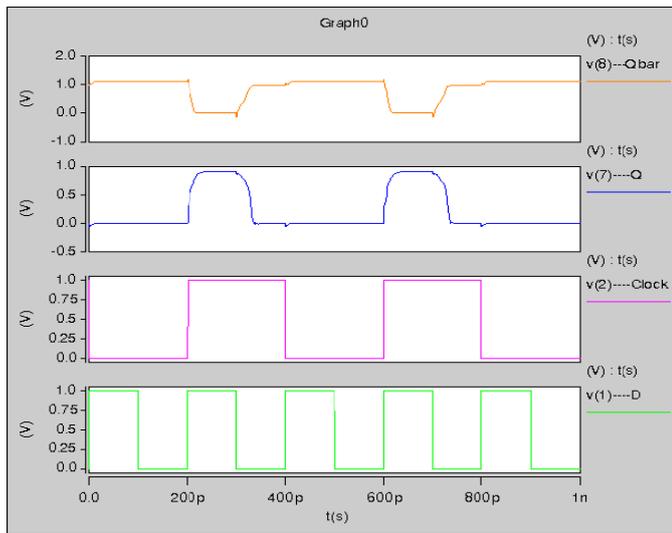Figure 8 shows the output waveform for design-III

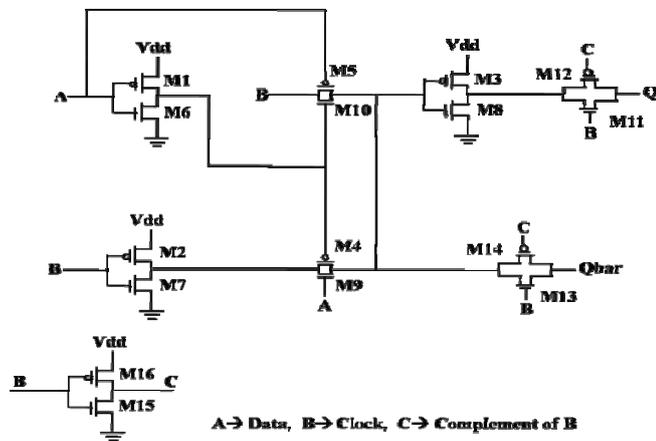Figure 8: Output for Design-III

2.4 D-Flip Flop Design-IV

Figure 9: D-flip flop design-IV

When AB=00, M1, M2, M5 gets ON. At this stage M1 produces output '1' which transfers M5 & M10 in ON condition and produces output B(0) as XOR output. XOR output is passed through inverter making XNOR output '1'. Since B (Clock) is off so Q will be previous value of output. When AB=01, M1, M7, M5 gets ON. At this stage M1 produces output '1' which transfers M5 & M10 in ON condition and produces output B(1) as XOR output. XOR output is passed through inverter making XNOR output '0'. Since B (Clock) is high so Q will be the value of A. When AB=10, M2, M6, M9 gets on, at this stage M6 produces output '0' which transfers M4 in ON condition. M2 produces output '1' which flows through M4 & M9 making XOR output '1'. XOR output is passed through inverter making XNOR output '0'. When AB=11, M6, M7, M9 gets on, at this stage M6 produces output '0' which transfers M4 in ON condition. M7 produces output '0' which flows through M4 & M9 making XOR output '0'. XOR output is passed through inverter making XNOR output '1'.

This is how the circuit works as a D-flip flop based on XOR/XNOR gate.

Table 5 shows the transistors characteristics at 32nm for design-IV.

Table5: Transistors Characteristics for Design-IV

MOSFET	W/L ratio
M1	0.469
M2	0.625
M3	0.375
M4	0.469
M5	0.500
M6	0.500
M7	0.344
M8	0.344
M9	0.469
M10	0.375
M11	0.344
M12	0.375
M13	0.375
M14	0.469
M15	0.344
M16	0.500

Figure 10 shows the output waveform for design-IV
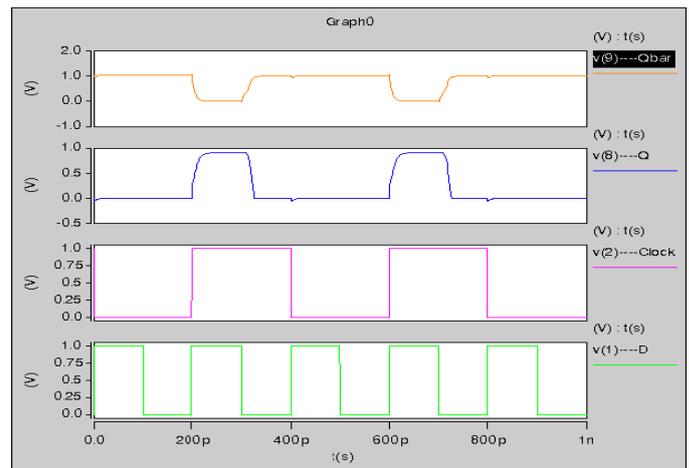
Figure 10: Output for Design-IV
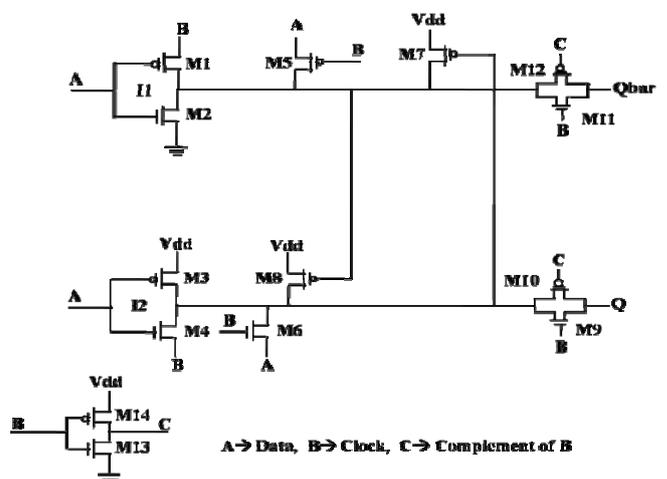
2.5 D-Flip Flop Design-V

Figure 11: D-flip flop design-V

MADHUR KULSHRESTHA et al.
DATE OF PUBLICATION: NOV 28, 2014

ISSN: 2348-4098
VOL 2 ISSUE 8 NOV-DEC 2014

When AB=00, M1, M3, M5 gets ON. At this stage M1 gives output B which flows upto XOR node making XOR output '0'. M3gives output '1' & XOR output switches M8 on which makes XNOR output '1'. Since B (Clock) is off so Q will be previous value of output. When AB=01, M1, M3, M6 gets ON. At this stage M1 gives XOR output B as '1'.M3 gives output '1' but due to M6 XNOR output becomes '0'. Since B (Clock) is high so Q will be the value of A. When AB=10, M2, M4, M5 gets on, at this stage M5 gives XOR output A as '1'. M4 gives output B(0) as XNOR output. When AB=11, M2, M4, M6 gets on, at this stage M2 gives output '0' as XOR output which switches M8 on and M6 also gives output '1' as XNOR output.

This is how the circuit works as a D-flip flop based on XOR/XNOR gate.

Table6 shows the transistors characteristics at 32nm for design-V.

Table 6: Transistors Characteristics for Design-V

MOSFET	W/L ratio
M1	0.563
M2	0.406
M3	0.375
M4	0.375
M5	0.438
M6	0.375
M7	0.500
M8	0.563
M9	0.438
M10	0.406
M11	0.406
M12	0.344
M13	0.406
M14	0.375

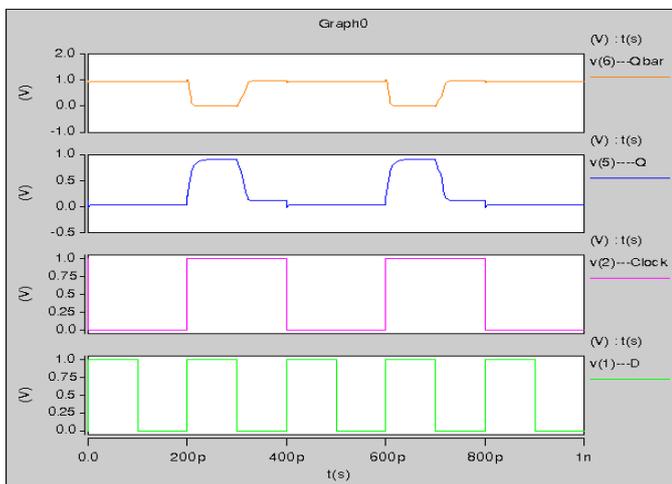Figure 12 shows the output waveform for design-V

Figure 12: Output for Design-V

3. RESULTS & SIMULATION

All designs are simulated using 32nm UMC CMOS technology for different values of Vdd. Comparison table for each design is mentioned below:

Table 7: Comparison table for design-I for different Vdd

No. of Transistors used = 14				
Parameters	Vdd=0.9V	Vdd=1V	Vdd=1.2V	Vdd=1.5V
Average Power (µW)	0.38	0.43	0.55	1.19
Delay time (ps)	204.95	205.16	205.78	207.03
PDP (fJ)	0.078	0.088	0.113	0.246

Table 8: Comparison table for design-II for different Vdd

No. of Transistors used = 16				
Parameters	Vdd=0.9V	Vdd=1V	Vdd=1.2V	Vdd=1.5V
Average Power (µW)	1.27	1.84	4.32	8.31
Delay Time (ps)	126.93	133.41	149.99	155.05
PDP (fJ)	0.16	0.25	0.65	1.29

Table 9: Comparison table for design-III for different Vdd

No. of Transistors used = 16				
Parameters	Vdd=0.9V	Vdd=1V	Vdd=1.2V	Vdd=1.5V
Average Power (µW)	1.69	2.12	3.59	12.52
Delay Time (ps)	217.07	216.94	222.23	255.87
PDP (fJ)	0.37	0.46	0.79	3.20

Table 10: Comparison table for design-IV for different Vdd

No. of Transistors used = 16				
Parameters	Vdd=0.9V	Vdd=1V	Vdd=1.2V	Vdd=1.5V
Average Power (µW)	0.63	0.75	1.03	2.77
Delay Time (ps)	213	212.95	213.41	212.94
PDP (fJ)	0.13	0.16	0.22	0.59

Table 11: Comparison table for design-V for different Vdd

No. of Transistors used = 14				
Parameters	Vdd=0.9V	Vdd=1V	Vdd=1.2V	Vdd=1.5V
Average Power (µW)	2.31	2.79	3.94	6.27
Delay Time (ps)	209.33	212.45	249.83	214.35
PDP (fJ)	0.48	0.59	0.98	1.34

These simulation results show that as we increase the power supply (Vdd), propagation time delay and power delay product increases. Through these tables I have shown the different parameters of each D-flip flop design based on XOR/XNOR circuit.

4. CONCLUSIONS & FUTURE SCOPE

In this thesis, I have designed different circuits of D-flip flop based on XOR/XNOR gate using CMOS inverters, NMOS digital switches, pass transistors and GDI cell. Each circuit structure has been designed using 32nm UMC CMOS technology. All the designs have been simulated in HSPICE and the results are checked for the voltage range from 0.9V to 1.5V and 25 degree centigrade. Design-I is considered to be the best optimized design of D-flip flop based on XOR/XNOR gate with average power = 0.38μW and power delay product (PDP) = 0.078fJ at Vdd = 0.9V. I have studied the comparison between different designs of D-flip flop based on XOR/XNOR gate circuits in detail. Thus for high speed microprocessors this best optimized design can be used to perform various arithmetic operations.

In future D-flip flop based on XOR/XNOR circuits can be designed more efficiently. As technology is getting advanced, power consumption, delay time, chip area are the main concern issues which we have to improve, therefore these circuits can be designed to solve these issues more efficiently to reduce the total cost of the system by optimizing transistors' sizes.

REFERENCES

1. J.M. Rabaey, A. Chandrakasan, B. Nikolic, "Digital integrated circuits: a design perspective", Prentice Hall, 2002.

2. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", 2003.

3. Neil H.E. Weste, David F. Harris, "CmosVlsi Design: A Circuits and Systems Perspective", 2005.

4. K. Roy and S. Prasad, Low Power CMOS VLSI Circuit Design.

5. Frank Schwierz, Hei Wong, Juin J. Liou, "Nanometer CMOS", Pan Stanford Publishing, 2010.

6. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", 2002.

7. Wayne Wolf, "Modern VLSI Design", Pearson Education 2nd Edition, 2007.

8. HSPICE User's Manual Meta-Software, 1996.

9. Hamed Sadeghi, Hamed Mohammadi Jirandeh, Ali Zakeri, "Improvement in Sub-circuit of Full Adder Cell (XOR and XNOR) by GDI and Fin FET Structure", International Journal of Scientific & Engineering Research, Volume 5, Issue 5, May, 2014.

10. Nabihah Ahmad, Rezaul Hasan, "A New Design of XOR-XNOR gates for low power application", International Conference on Electronic Devices, Systems & Applications, 2011.

BIOGRAPHY

Madhur Kulshrestha, is a final year student of M. Tech(Dual Degree) EC+VLSI from Gyan Vihar School of Engineering and Technology Jaipur, Rajasthan, India.

Vipin Kumar Gupta received the B.E. Degree in Electronics and Communication from Sri Balaji College of Engineering and Technology Jaipur in 2008 and M.Tech in VLSI Design from MNIT Jaipur in 2011.Currently Assistant Professor at Suresh Gyan Vihar University in EC Deparment.